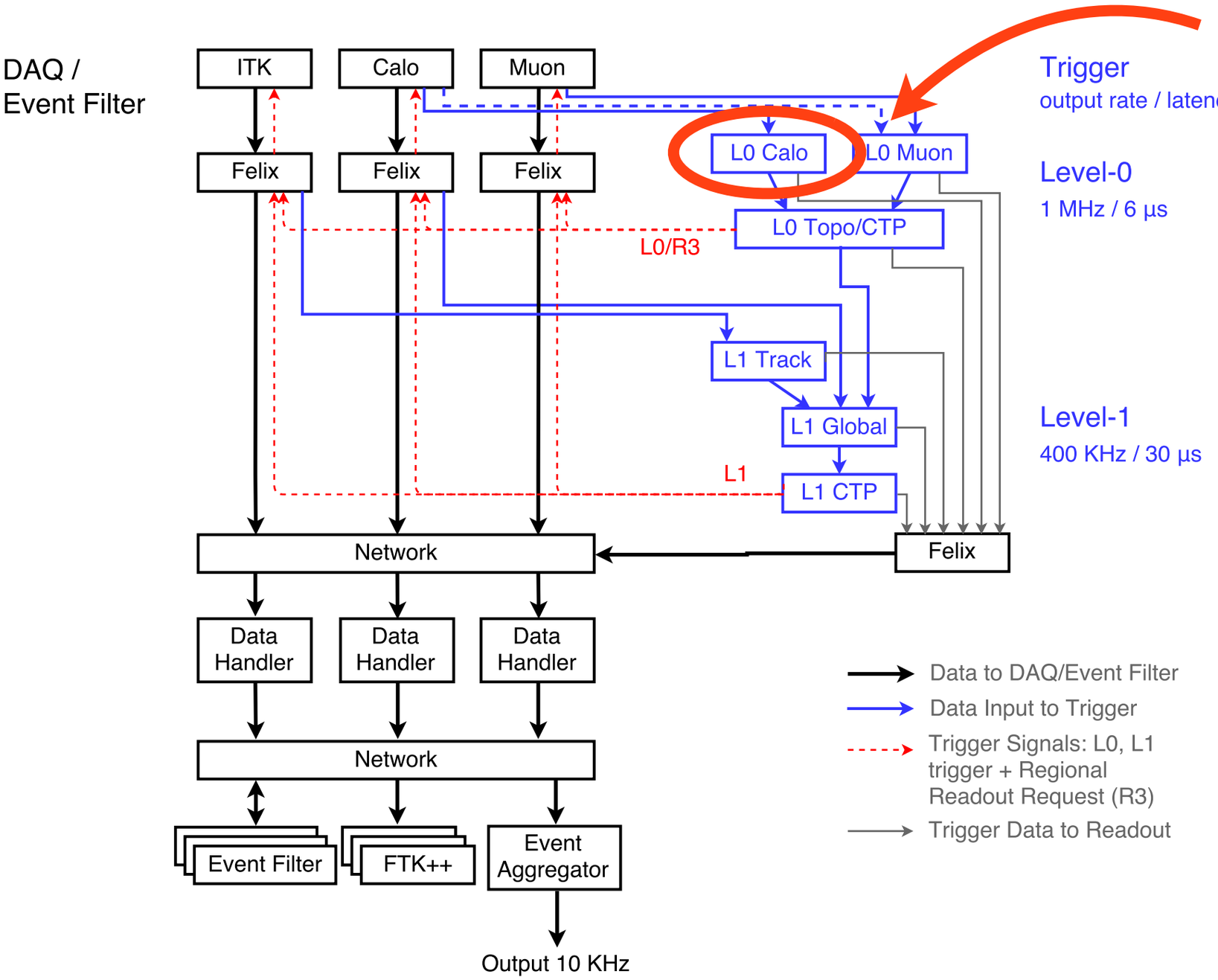
TDAQ Scrubbing

Outline

- Overview of system components and proposed US contributions
- WBS Structure
- Summary of Budget + Profile
- Review of BoEs - line by line
- L0Calo scope contingency
- RoID scope contingency
- What if the architecture changes to single-level?
- Profile and NSF preproduction

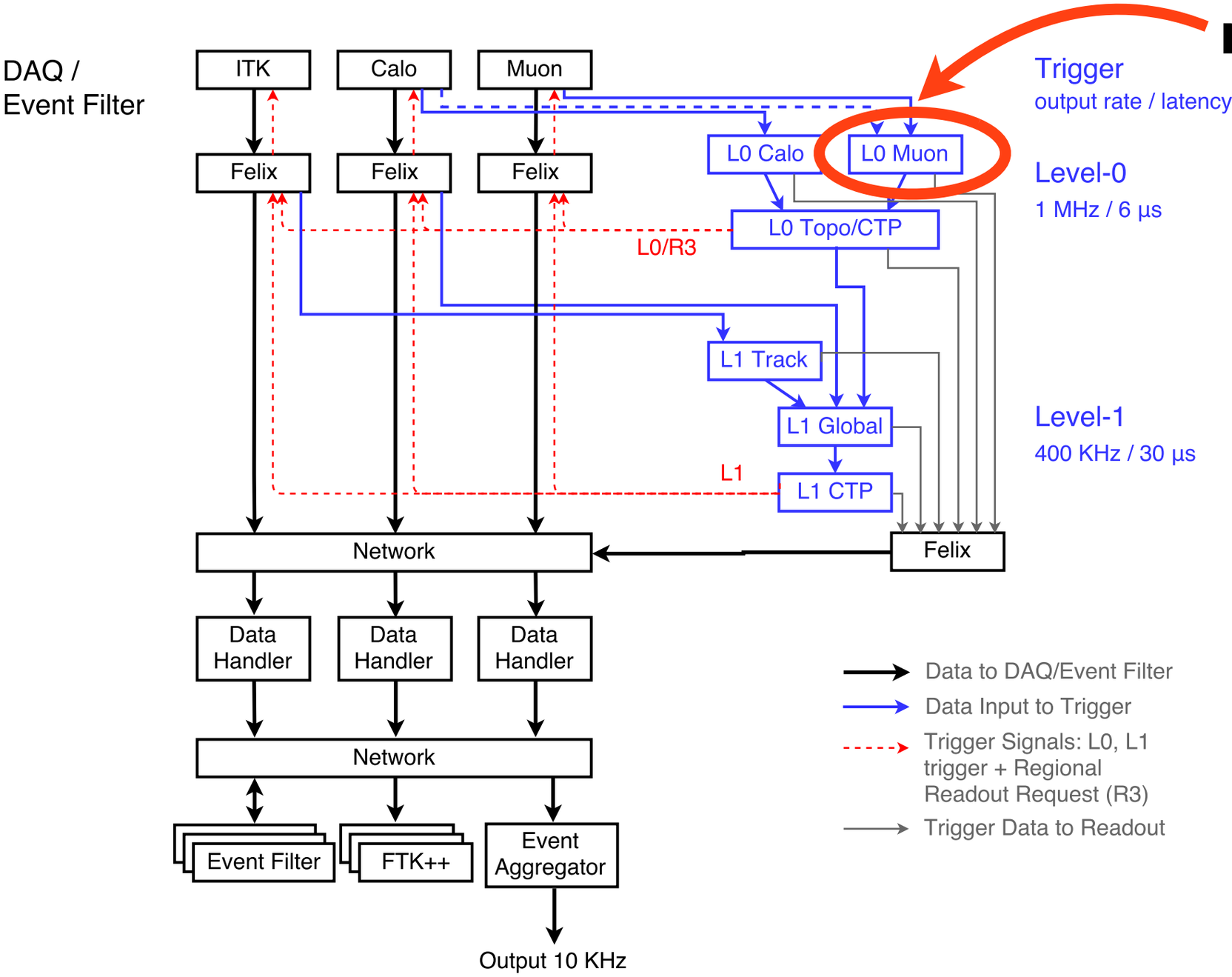
Overview of the System



Migration of Phase-I US deliverables

- Tile input to L0Calo will to new digital input from Tile preprocessor
- New Tile **Optical plant** needs to be built because of the new Tile Front-end electronics
- **gFex firmware** needs to be upgrade for
  - new Tile input,
  - possible new algorithms for higher pile-up / new input
  - New output requirements for L0Topo and DAQ

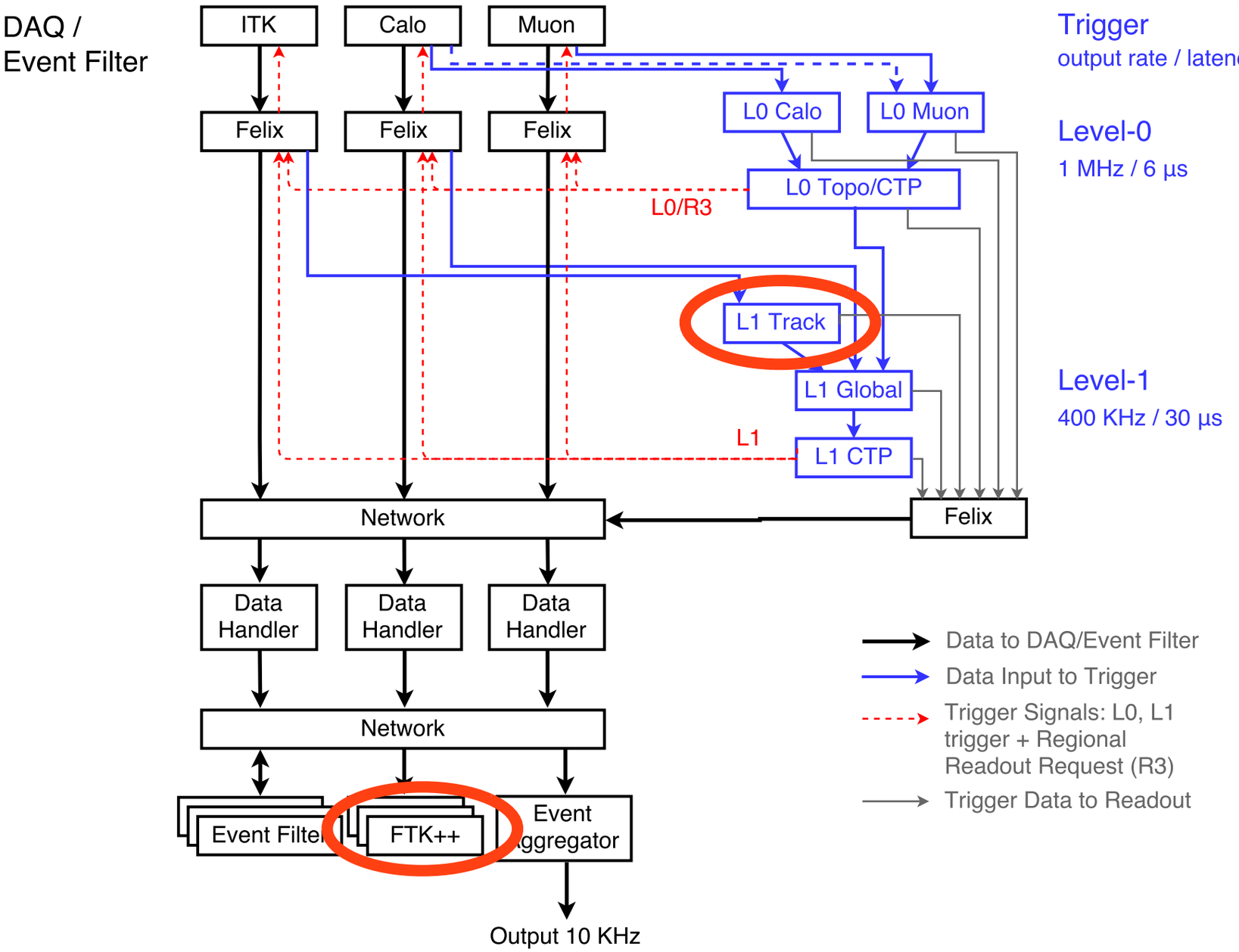
Overview of the System



New MDT trigger

- Proposed US deliverable (in TDAQ) is the pattern recognition
- Irvine is proposing to build a mezzanine with FPGA with firmware for segment finding and track fitting

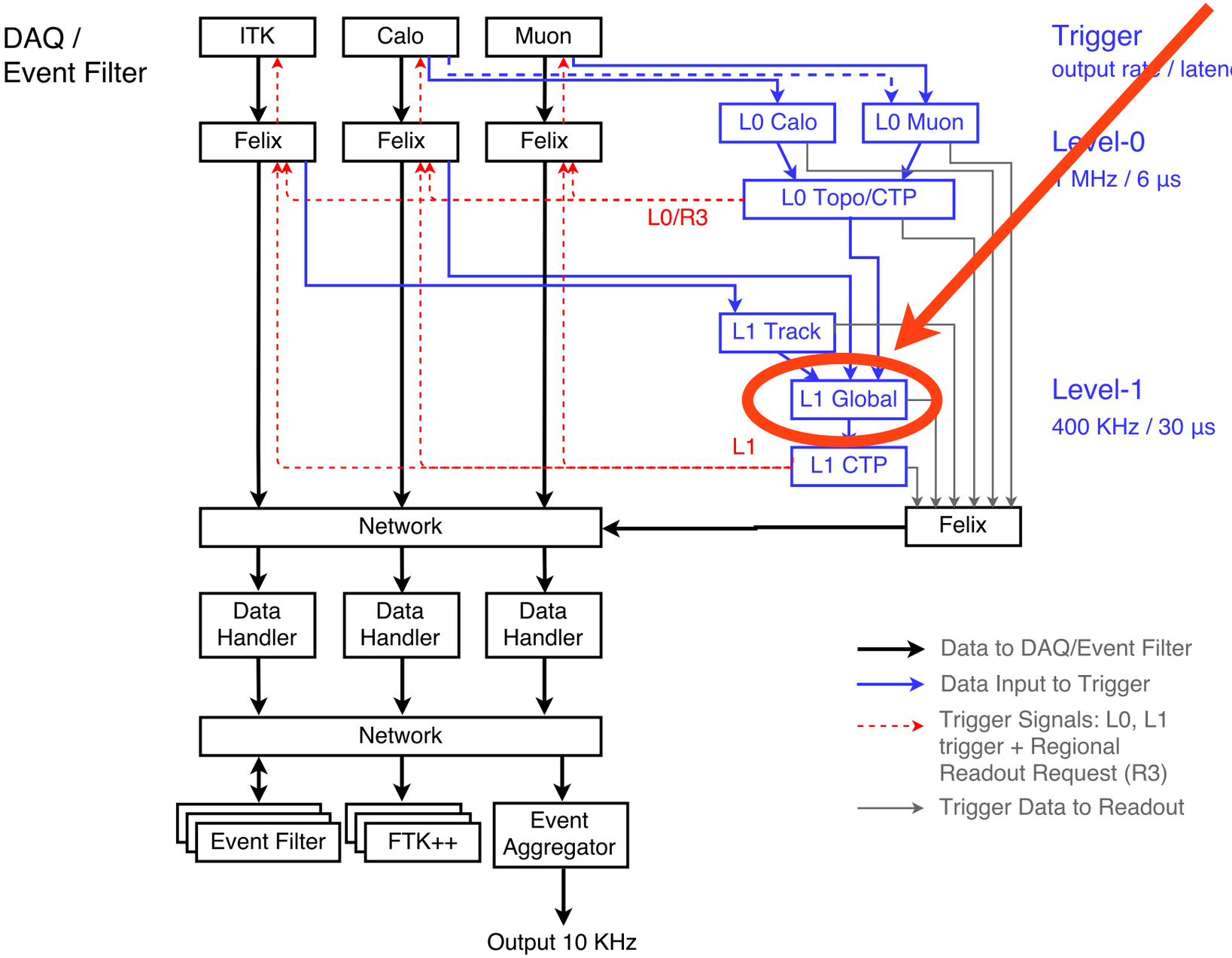
Overview of the System



L1 Track and FTK++

- 8 interested institutes:
  - Argon, Chicago, Indiana, NIU, Penn, Stanford, SLAC, UIUC
- Follow Scoping Doc assumption common hardware for L1Track/FTK++
- Deliverables/Items
  - **Mainboard** with firmware
  - **Mezzanine for track fitting**
  - **High-speed data input**
    - Transition module
    - Data handling firmware

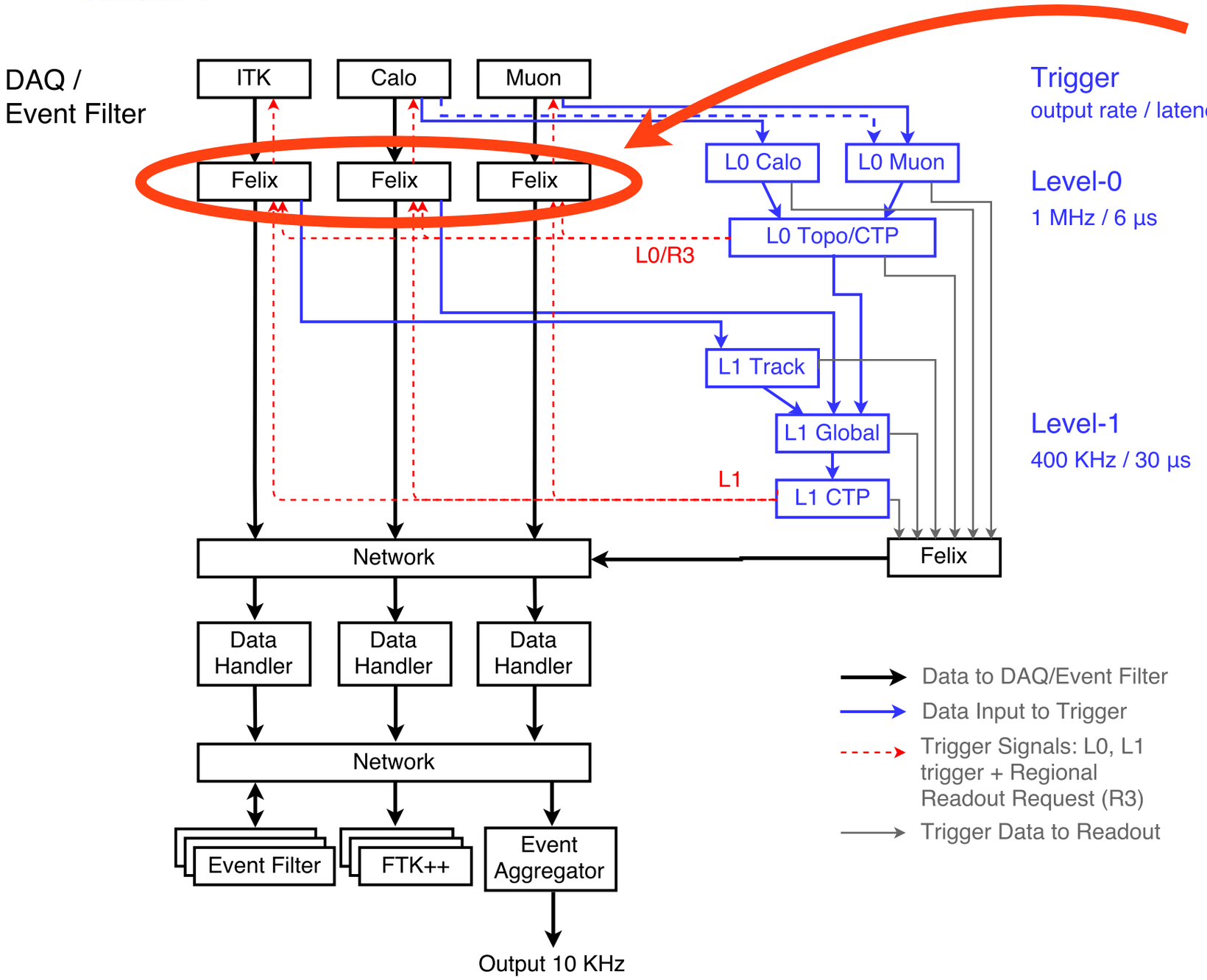
Overview of the System



L1 Global

- 7 interested institutes:
  - Brookhaven, Chicago, Indiana, LSU, MSU, Oregon, Pitt
- Deliverables
  - **Aggregator** with firmware
  - **Hadronic Trigger algorithm firmware**

Overview of the System



- Front-end Exchange Link
- Common dedicated front-end link to commercial network connection for all subsystems
- Deliverable is **Felix board** with firmware

WBS Structure

WBS		Deliverable	Funding	Institutes
6.7	**DAQ/Data Handling**			
	6.7.y.1	L1Global Aggregator	DOE	BNL
	6.7.y.2	L1Track/FTK++ Data Handling	DOE	ANL, SLAC
	6.7.y.3	DAQ/FELIX	DOE	ANL, BNL
6.8	**Trigger**			
	6.8.y.1	L0Calo	NSF	Indiana, MSU
	6.8.y.2	L0Muon	NSF	Irvine
	6.8.y.3	L1Global Firmware	NSF	Chicago, Indiana, LSU, MSU, Oregon, Pitt
	6.8.y.4	L1Track/FTK++ Processing	NSF	Indiana, Penn, Chicago, Illinois, NIU, Stanford

NSF Items

WBS	Deliverable/Item	Funding	Institutes
6.8.y.1	**L0Calo**	**NSF**	
	gFEX Firmware		Indiana
	Optical Plant		MSU
6.8.y.2	**L0Muon**	**NSF**	
	MDT Trigger		Irvine
6.8.y.3	**L1Global**	**NSF**	
	Topo Clustering		MSU, Oregon
	Hadronic calorimeter object reconstruction		Chicago, Indiana, LSU
	Track-based pile-up rejection		Pitt
6.8.y.4	**L1Track/FTK++**	**NSF**	
	Main Board (HW & FW)		Indiana, Penn Chicago, Illinois, NIU Stanford
	Second Stage Board (HW & FW)		
	Data Formatting Firmware		

NSF Items

WBS	Deliverable/Item	Funding	Institutes
6.7.y.1	**L1Global Aggregator**	**DOE**	
	Aggregator		BNL
6.7.y.2	**L1Track/FTK++ Data Handling**	**DOE**	
	L1Track/FTK++ Data Handling		ANL, SLAC
6.7.y.3	**DAQ/FELIX**	**DOE**	
	FELIX Boards		ANL, BNL

NSF

Deliverable	Item	Core (k$)	FTE Sum	Labor	Travel	M&S	Total Cost
NSF							
L0 Calo	Optical Plant	41	0.8	93		41	134
L0 Calo	gFEX firmware		1.7	313	5	5	323
L0 Muon	Fitting Mezzanine + Firmware	461	12.3	2,149	49	526	2,724
L1 Global	Algorithm Firmware		12.0	2,271	60	222	2,553
L1 Track/FTK++	mainboard (hardware and firmware)	3,600	7.0	1,400	54	3,622	5,076
L1 Track/FTK++	Second stage hardware + firmware	2,094	7.0	1,400	54	2,159	3,613
Summary							
Total NSF		6,196	40.7	7,282	222	6,575	14,423
JOG Guidance		6,868					13,858

Production vs Preproduction later (doesn't appear to be an issue)

Sum BoEs some more that expect, some less balance ends up close to guidance

Later slides go through this line by line

DOE

Deliverable	Item	Core (k$)	FTE Sum	Labor	Travel	M&S	Total Cost
DOE							
L1 Global	Aggregator	916	7.3	848	37	1,154	2,039
L1 Track/FTK++	Data Input	2,400	4.5	1,878	12	2,426	4,316
DAQ	FELIX cards	1,000	11.3	2,618	100	1,120	3,838
Summary							
Total DOE		4,316	23.1	5,344	149	4,700	10,193
JOG Guidance		1,628					5,201

Jog Numbers

Item	Core	DOE Total
L1 Global	-	248
L1 Track	-	280
FTK++	-	-
DAQ/EF	1,628	4,672

- FELIX slightly less than JOG
- L1 Global Aggregator and L1 Track/FTK++ high to include data handling hardware in DOE

Later slides go through this line by line

L1 Global Aggregator

BOE from Michael Begel ***Institutes: BNL***

General Description

- 100 to 300 input sources to the global system (24 (8?) boards)
  - Depending on whether links from the calorimeter RODs to Global are located on mezzanines or main modules
  - Each of these sources needs to have a route to every Event Processor.
  - Requires low- latency and high I/O which is best realized in large FPGAs
  - Work includes design, construction, and testing of the DAG board as well as development of input, output, and board control firmware.

Tag	Stage	FY	Labor FTE	Labor Hrs	Labor $	M&S $	Travel $	Total $
DAG1000	*Design*	18	0.25 Jr. Eng	444	$26,062.00	$0.00	$0.00	$26,062.00
DAG1010	*Prototype 1*	19	2.0 Jr. Eng	3552	$224,460.00	$54,000.00	$11,500.00	$289,960.00
	Prototype 2	20	2.0 Jr. Eng	3552	$233,438.00	$110,000.00	$10,000.00	$353,438.00
DAG1020	*Pre-production*	21	2.0 Jr. Eng	3552	$240,442.00	$110,000.00	$10,000.00	$360,442.00
DAG1030	*Production*	22	1.0 Jr. Eng	1776	$123,827.00	$880,000.00	$5,500.00	$1,009,327.00
	Total $				$848,229.00	$1,154,000.00	$37,000.00	$2,039,229.00

ATLAS core = $916k = 100%

FELIX

BOE from Jinlong and Chen ***Institutes: ANL, BNL***

- Contribution at a similar level as in Phase-I
- Hardware and firmware for next generation of FELIX board for ATLAS TDAQ Phase-II upgrade
- Design, prototype and production
- Production of a fraction of the total FELIX cards (~20% of FELIX core cost)

	Materials [$]	Travel [$]	Engineer [hr]	Tech [hr]	Labor [$]
Design	80,000	40,000	7992	0	1,023,452
Prototype	540,000	40,000	7104	1776	1,165,287
Production	500,000	20,000	2309	888	429,842

ATLAS core = ~1000k = 20%

L1Track/FTK++ Overview

Two systems with assumed common hardware

Each system has

- Mainboard supports two kinds of mezzanines (propose design and 50% core)
  - data handling/formatting/preprocessing
- RTM to handle network connections (propose design and 50% core)
- Mezzanines:
  - Pattern recognition: AM chip , FPGA for "first-stage" fitting (No US involvement)
  - Second stage fitting: track fit to ~offline quality (propose 100% hardware and firmware)

Core fraction within ATLAS

- Can we propose 100% of design for main board + RTM, but only 50% core?
- Possible Argument
  - Main board core is larger fraction of core than the design is fraction of design work
  - We are proposing ~50% of core and ~50% of effort
    US effort = main board w/RTM + mezzanine
    non-US effort = AM chip + mezzanine

L1 Track/FTK++ RTM

BOE from Mel

Institutes: ANL, SLAC

Rear Transition Module (RTM) (US cost 50% of core, 100% design)

Hardware only

Engineer	2 FTEs	$400k
Technician	0.5 FTEs	$65k
Travel	4 trips	$12k
M&S		$2.4M

Add firmware for data handling

- 2 FTEs at average of SLAC and ANL engineer labor rates = $930k

QSFP Issue (QSFP = quad fiber connector)

- Mel believes Scoping Document left out the cost of QSFPs (also left out in FTK)
  - Checking with TDAQ management...
- This could add $4M to the core! (50% US = $2M)
- Need to check fiber count!

ATLAS core = $800k???

Not corrected for QSFPs

Net effect, this is $3M of the $5M we are over in the DOE guidance

Mainboard

BOE from Mel

Institutes: Subset of Indiana, Penn, Chicago, Illinois, NIU, Stanford

Mainboard (US cost 50% of core, 100% design)

Hardware and firmware

SD says 1380 boards!

Engineer	6 FTEs	$1.25M
Technician	1FTEs	$140k
Travel	18 trips	$54k
M&S		$3.6M

ATLAS core = $3.6M = 50%

Mel costed with 4 student FTEs

- These were removed for 2 Eng FTEs (with some assumed help from students)

Also added some test hardware to M&S

- Tiny compared to core

Second Stage Mezzanine

BOE from Mel

Institutes: Subset of Indiana, Penn, Chicago, Illinois, NIU, Stanford

Second stage mezzanine
(US cost 100% of core, 100% design)

Hardware and firmware

Engineer	6 FTEs	$1.25M
Technician	1FTEs	$140k
Travel	18 trips	$54k
M&S		$2.1M

ATLAS core = $2.1M = 100%

Mel costed with 4 student FTEs

- These were removed for 2 Eng FTEs (with some assumed help from students)

Also added some test hardware to M&S

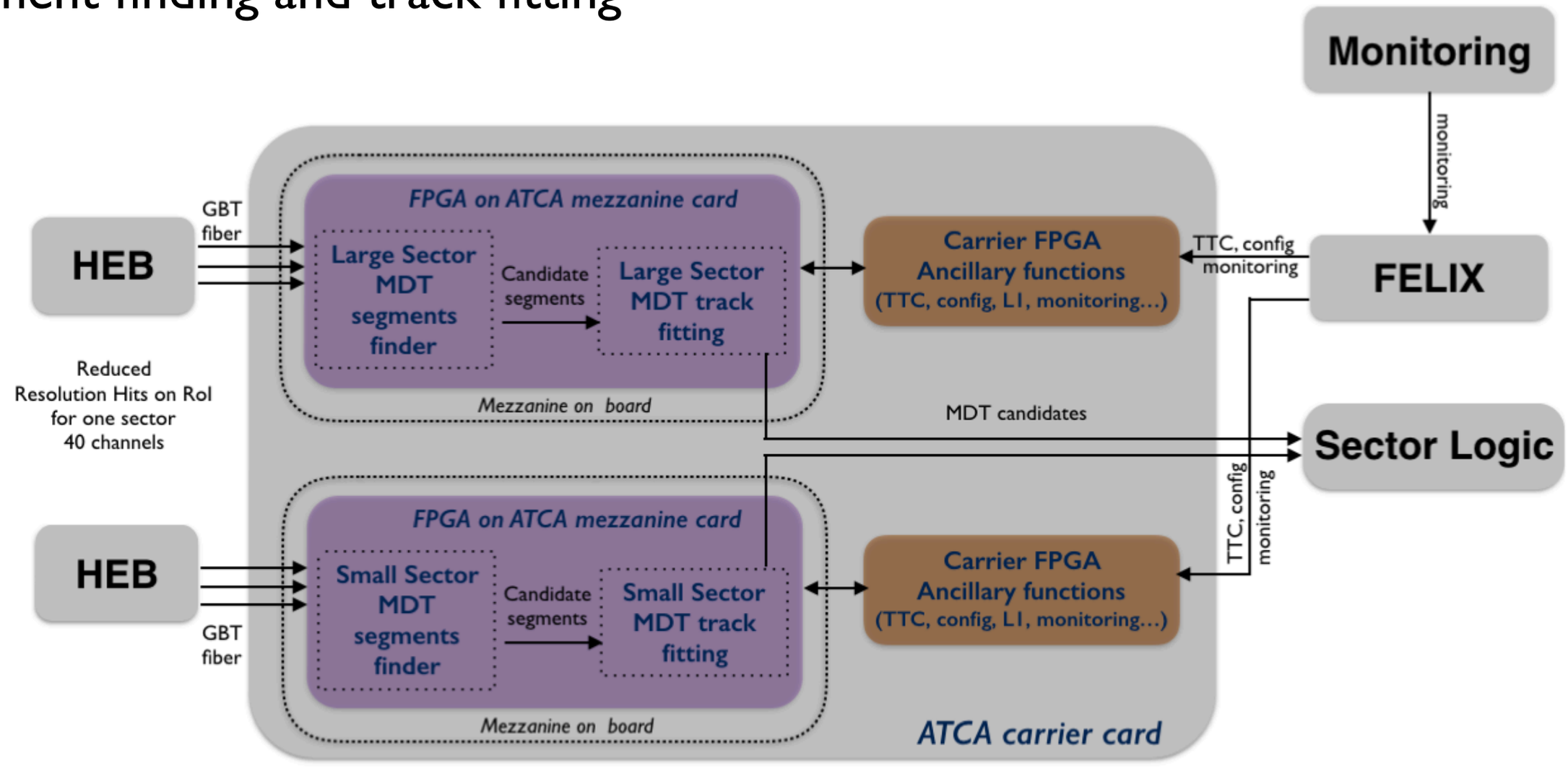
- Tiny compared to core

MDT Trigger

BOE from Anyes

Institutes: Irvine

Segment finding and track fitting



MDT Trigger

BOE from Anyes

Institutes: Irvine

ATLAS core = $461k = 30%

	FTE
Engineer	7
Tech	2.5
Eng Student	4.5

6.x.2 MDT Trigger Hardware	Labor Hrs	Labor $	M&S $	Travel $	Total $
6.x.2.1 Firmware+AMC Design & Prototype	**11544**	**$1,019,879**	**$60,397**	**$26,170**	**$1,106,446**
Assoc Projc Sci	1776	$156,725			
Engineer	7104	$787,797			
Student	2664	$75,357			
M&S			$60,397		
Travel				$26,170	
6.x.2.2 Firmware+AMC Preproduction	**5772**	**$421,577**	**$46,939**	**$15,361**	**$483,877**
Engineer	2220	$258,080			
Technician	1332	$98,303			
Student	2220	$65,194			
M&S			$46,939		
Travel				$15,361	
6.x.2.3 Firmware+AMC Production & testing	**9324**	**$711,034**	**$424,777**	**$17,749**	**$1,153,560**
Engineer	3108	$378,199			
Technician	3108	$237,298			
Student	3108	$95,537			
M&S			$17,820.79		
Construction			$406,956.52		
Travel				$17,749	
MDT Trigger hardware	**26640**	**$ 2,152,489**	**$ 532,114**	**$ 59,280**	**$ 2,743,883**

L1 Global Algorithms

BOE from Elliot

Institutes: Chicago, Indiana, LSU, MSU, Oregon, Pitt

General Theme: Hadronic Triggering

Costing based on gFEX experience ~ 2 FTE/algorithm

ATLAS core = $0

- Topoclustering is novel and requires iterate counts as 2 algs
- 1 demonstrator and ~3 prototype boards for testing (too expensive to have 1 board/institute

	Labor Hrs	Labor $	M&S $	Travel $	Total
6.8.y.3 L1 Global Firmware	21,120	$2,271,638	$222,000	$60,000	$2,553,638
Topoclustering					
Engineer	7120	$757,213	$75,000	$20000	$851,213
Jet Finding					
Engineer	3560	$378,606	$37000	$10000	$425,606
Fat-jet Reconstruction					
Engineer	3560	$378,606	$37000	$10000	$425,606
Global Quantities					
Engineer	3560	$378,606	$37000	$10000	$425,606
Track-based pile-up rejection					
Engineer	3560	$378,606	$37000	$10000	$425,606

Lot's of additional scope interest: Monitoring, Framework, Taus

gFEX Firmware

BOE from Hal

Institutes: Indiana

gFex firmware needs to be upgrade for

- new Tile input,
- possible new algorithms for higher pile-up / new input
- New output requirements for L0Topo and DAQ

ATLAS core = $0

	Labor Hrs	Labor $	M&S $	Travel $	Total $
6.8.y.1 L0 Calorimeter					
gFEX Firmware (Indiana)	**2,975**	**$312,629**	**$5,000**	**$5,000**	**$322,629**
Engineer	2,975	$312,629	$5,000	$5,000	$322,629

Optical Plant

BOE from Reinhard

Institutes: MSU

Detailed BoE costs seems very clear

ATLAS core = $41k =100%

Item	Cost per	# of items	Total cost
MTP cable	$100	120	$12,000
MTP breakout cable	$40	12	$4,800
Mapping module	$4,500	5	$22,500
Enclosure	$500	1	$500
Misc parts			$1,200
Total			$41,000

Task Name	**Effort (person-months)**	**Calendar Duration**
Engineering Specification	1	6
Design	3	18
Acceptance Tests	2	6
System Tests	2	6
Project Review Preparation	1	12
Project Total:	**9 (0.75 FTE)**	**36 (total duration)**

RoID

TDAQ WBS 1.1.3 in the Scoping Document

- A critical component to merge the RoIs and translate to detector module map then to send via low latency link
- US expertise and encouragement of TDMT
- Well fit in the "Data Handling" area
- Zeroed out in the JOG reference sheet

The information in the earlier WBS

			CORE Cost	Fraction of	Total Cost
WBS	**Item**	**Institutes**	**(AY k$)**	**ATLAS CORE**	**(AY k$)**
6.7	**TDAQ system**				
6.7.1	**Detector Data Handling**				
6.7.1.1	RoI Distributor	ANL	**225**	**100**	**1,226**

L0 Global/Topo

Potential additional scope beyond "Scoping Document"

The 1 MHz L0 rate was originally designed for 5e34 luminosity

- For contingency, 7e34 numbers were used in drafting constraint
- We are not planning to run up to 7.5e34 which means we have a -7% contingency (not counting pile-up effects)
- Also the hadronic thresholds for 4-jet, HT, and MET degrade significantly from the Run 1 menu

It is likely that new L0 Calo will be proposed within ATLAS

- There are many ideas that range significantly in cost an complexity
  - L1Global like "time-multiplexed" system
  - New tower construction in LAr and Tile preprocessors
  - I'm sure more are to come...
- There is significant interest in this topic in the US: ANL, BNL, Chicago, Oregon, Penn

In addition the current L1 Topo is oversubscribed

- Phase-1 L1Topo will become Phase-2 L0Topo (not clear if this will be oversubscribed)
- In some designs the Topo architecture is significantly rethought

Single Level Trigger

The original L0/L1 architecture was based on the assumption that some detectors would not be able to readout at greater than a few 100 kHz

- Strips in particular has increased its expect readout by 8x (or more)
  - This is partly due to the shift in the HL-LHC schedule
- Now nearly all the detectors will be able 1 MHz
  - Exception maybe some MDT chambers were the electronics is hard to replace
  - Also NSW is not clear yet

If all detectors can readout at 1 MHz the motivation for a split-level trigger is gone and we can move to a single level trigger

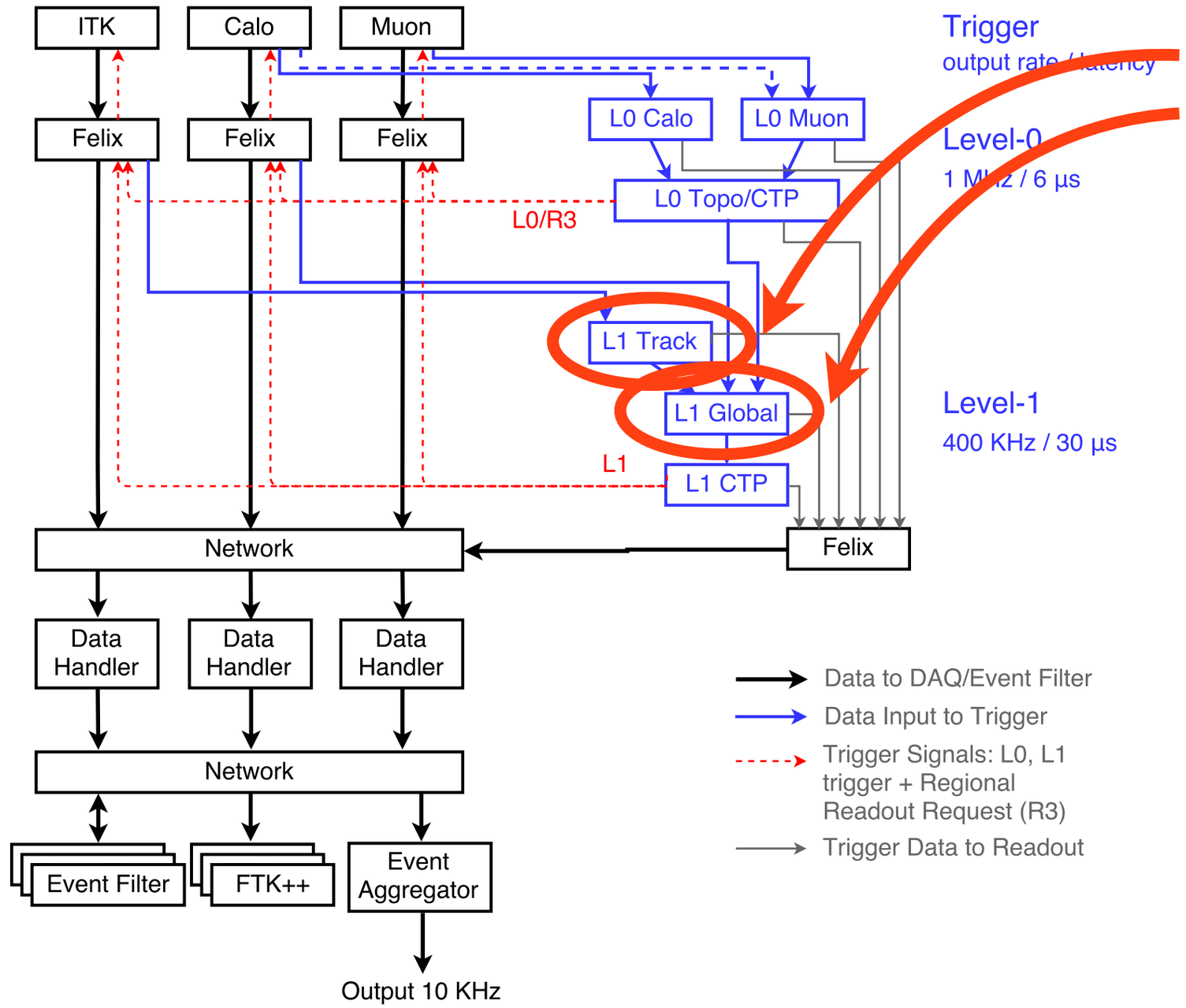
- Kevin (upgrade coordinator) is pushing strongly to see this realized

The draft TDAQ IDR is being updated to include the single-level option

So what would we do...

Single Level Trigger

DAQ /
Event Filter



These go away

Single Level Trigger

L1 Track

- There will still be a need to do region of interest tracking at 1 MHz in ~10% of the detector
- This will be stated in the TDAQ IDR
- The L1 Track functionality could be integrated into the FTK++ or it could remain a separate system functioning as a preprocessor to the EF

Cost impact of L1 Track just being removed

- Common FTK++/L1 Track hardware means hardware development cost unchanged
- L1 Track fraction of core is ~30% so reducing US core contribution by 30% would be $1.7M to $2.4M depending on understanding of QSFPs in core
- Unlikely to really happen
- At this point, design changes could easily effect costs on that scale without a change in architecture

Single Level Trigger

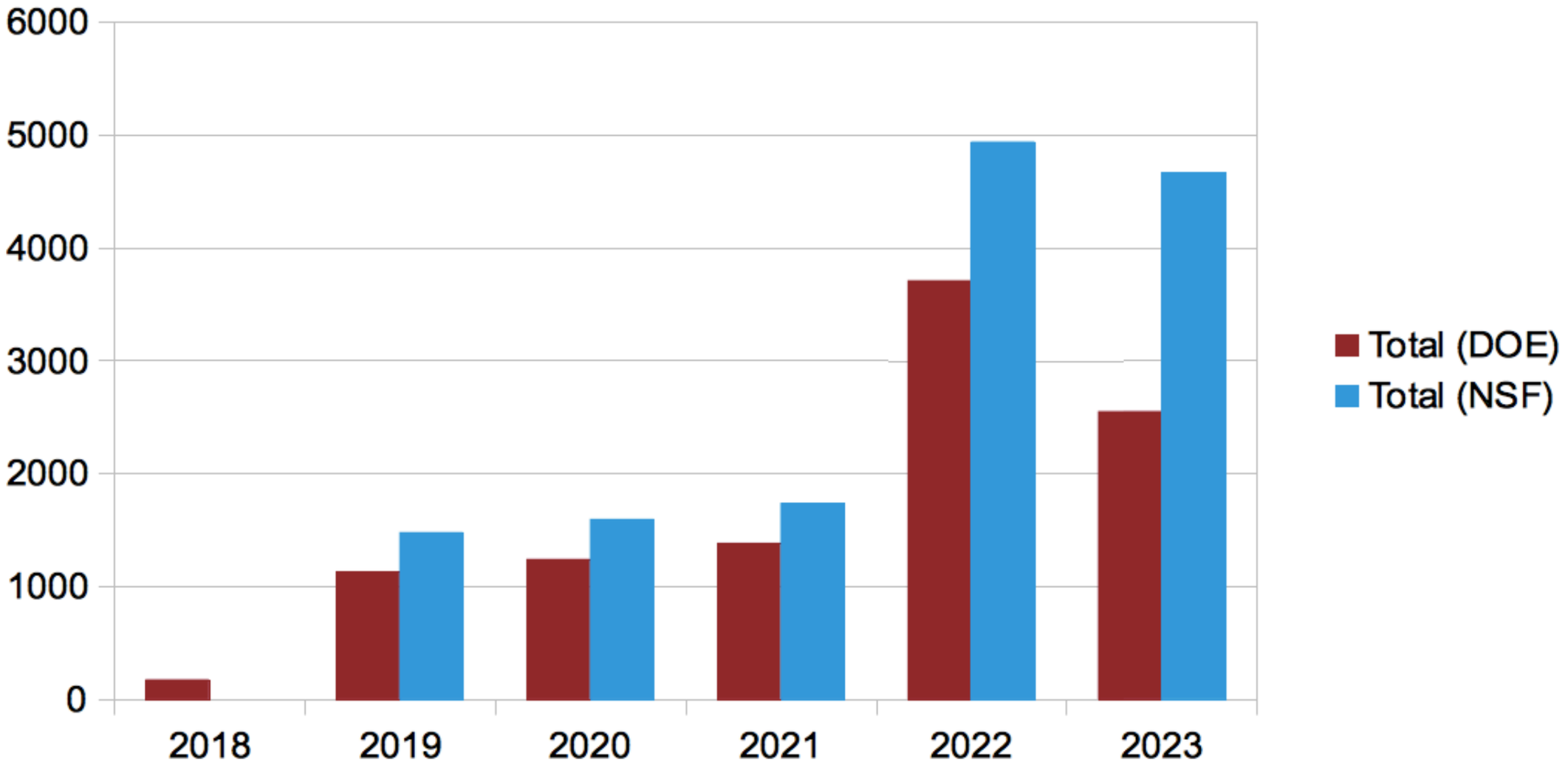
L1Global

- The L1Global functionality to process high granularity calorimeter information at a high rate is still needed, but it could take a very different form, e.g.:
  - Preprocessing in LAr and Tile preprocessors
  - GPU/CPU(?) processing in augmented EF farm
  - Move L1Global to L0Global
    - Addresses previously mentioned possible L0 Calo scope change

Guesses

- A shift to a single level trigger and the removal of L1Global will probably be taken at the ATLAS level as an opportunity to increase the L0 scope
- It would be natural for the US program to follow that
- Costs could be significantly different, e.g. L0Global
  - 1 MHz → 40 MHz
  - 20μs latency → <10μs latency
  - No track input → fewer algorithms?

Profile



Not all BoEs gave a full profile. For those that didn't provide we spread manpower evenly over 5 years, escalated costs, and split production over last two years (test systems in first year)

NSF Preproduction

Deliverable	Item	Preproduction	Assumptions
NSF			
L0 Calo	Optical Plant		25% Effort ~ 2 out of 9 FTE months – consistent with Reinhard's schedule
L0 Calo	gFEX firmware	42	20% Manpower + $5k licenses + 1 trip to CERN
L0 Muon	Fitting Mezzanine + Firmware	363	Anyes' estimate
L1 Global	Algorithm Firmware	482	20% Manpower + $42k hardware for demonstrator boards and $12k travel
L1 Track/FTK++	mainboard (hardware and firmware)	285	20% Manpower + $11k hardware for two test mainboards
L1 Track/FTK++	Second stage hardware + firmware	307	20% Manpower + $33k hardware for four test mainboards + 4 mezzanines
Summary			
Total NSF		1,479	
JOG Guidance		1,630	

Not all BoEs gave a full profile, for pre-production the rough assumption is 20% of manpower plus a test stand